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**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Docket Number (Optional)

2000.002500

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on August 17, 2007Signature Typed or printed name Jaison C. John

Application Number

09/225,388

Filed

01/05/1999

First Named Inventor

David W. Smith

Art Unit

2616

Examiner

Nguyen, Toan D.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

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applicant/inventor.

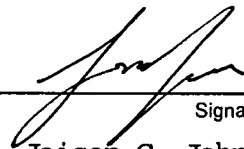
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assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.  
(Form PTO/SB/96)

☒

attorney or agent of record.

Registration number 50,737

Signature

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Typed or printed name

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Telephone number

☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 \_\_\_\_\_

Date \_\_\_\_\_

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.  
Submit multiple forms if more than one signature is required, see below\*.

☒\*Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:  
DAVID W. SMITH

Group Art Unit: 2616

Serial No.: 09/225,388

Examiner: Toan D. Nguyen

Filed: JANUARY 05, 1999

Conf. No.: 2528

Atty. Dkt.: 2000.002500/TT2581

For: METHOD AND APPARATUS FOR  
PATTERN MATCHING ON SINGLE  
AND MULTIPLE PATTERN  
STRUCTURES

CUSTOMER NO.: 23720

**REMARKS CONCERNING PRE-APPEAL BRIEF**  
**REQUEST FOR REVIEW**

**MAIL STOP AF**

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37 C.F.R. 1.8

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August 17, 2007  
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Sir:

Applicant submits the following remarks concerning the Pre-Appeal Brief Request for Review and Notice of Appeal filed concurrently herewith.

After a lengthy bout of prosecution, after many opportunities and exhausting many rejections, the Examiner for the first time asserted a rejection under 35 U.S.C. 112. Applicant respectfully asserts that the Examiner erred in maintaining the rejection of claim 1-35 under 35 U.S.C. 112. In the Final Office Action, the Examiner rejected claims 1-35 under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement as containing subject matter not described in the Specification. However, there is sufficient disclosure in the originally filed specification to enable all features of claims of the present invention.

Contrary to Examiner's remarks in the Final Office Action dated May 12, 2007, Applicant respectfully asserts that claims 1-35 do indeed comply with the enablement requirements under 35 U.S.C 112. In the previous office action, the Examiner asserted that independent claims 1, 10, 23, 32 and 34 are directed to detecting and decoding data comprising detecting the size of the data signals to use as a factor for decoding the data and decoding the receives that are data signals, ant that the disclosure does not support these elements. Applicant respectfully disagrees. In response to the Applicant citing various exemplary portions of the specification to show support of all of the elements of the claims, the Examiner asserted that the disclosure does not provide enablement as to how and which component or element explicitly detects a size of received set of signal. Applicant respectfully disagrees. Those skilled in the art would readily decipher the various exemplary components that perform the various steps recited in the claims. For example, the specification clearly discloses that the counter 240 increments the work count number, which may be indicative of the size of the data. *See Specification*, page 14, lines 6-10. The Specification also discloses that the host circuitry 150 can predetermine the composition of the data packets stored in memory. *See Specification*, page 14, lines 20-22. Still further, the Specification discloses that the mask circuitry [0 - n] 270 can facilitate the selective clocking of data comparison results, by checking the status of an extra bit that is transmitted in the data packets. *See Specification*, page 17, line 22-24. These exemplary components perform various steps called for by claims of the present invention, thereby properly enabling all aspects of the present invention. Applicant respectfully asserts that these are examples, and the various scopes of the claims are not limited to the disclosed embodiments. Those skilled in the art, upon a reading of the present patent application, could readily decipher the various components that are capable of performing the steps called for by claims of the present invention. Accordingly,

the Examiner erred in the Final Office action dated May 12, 2007 in rejecting the claims for allegedly lacking enablement.

The Specification clearly supports all of the elements of claims of the present invention. For example, Applicant respectfully directs the Examiner's attention to page 14, lines 1-23 of the Specification. In this example, the specification clearly notes that a serial to parallel converter and the data formatter receives data and converts to a serial stream into parallel format. *See* Specification, page 14, lines 4-5 of the Specification. The data formatter 220 uses a serial clock signal to convert it to a parallel word clock on a line 217. *See* page 14, lines 6-7. The word clock signal on the line 217 then increments the word count number in the counter 240, wherein the word count number is set to the address input of the memory elements [0-N] 330. *See* page 14, lines 6-10. The Specification discloses that known data value or expected data patterns can be programmed into the memory elements [0-N] 330. *See* Specification, page 13, lines 15-17. The Specification discloses that the a change in the word count number sent to the memory element 330 prompts the next set of possible matching frame of data is extracted from memory. *See* page 14, lines 12-13. Utilizing the comparators 320-326, the host interface 245 can predetermine the composition of the data packets, which should match any data packets that are addressed to that particular host. This stored data, as well as incoming data, may be used by the comparators 260 to determine if the respective data sets match. *See* Specification, page 14, lines 13-23. These steps, which utilize the size of the data, (*e.g.*, implementing the word count number and the counter 240), along with various logic gates and comparators), determine whether the value of signal indicating a proper match has been found and, if so, then the byte portion of the data latched. *See* Specification, page 14, line 22- page 16, line 7.

Yet another example of the size of the data being used to perform the detection and decoding of the data, in support of the claims is provided on pages 17-18 of the Specification.

The Specification discloses that in one embodiment, an extra bit per byte, affecting the length of the data frame, is transmitted. *See* Specification, page 17, line 25-page 18, line 1. The Specification discloses that the data detector/decoder 130 will receive data sets that have a size of  $n$  by 9, instead of  $n$  by 8. *See* Specification, page 18, lines 1-3. This extra bit will indicate whether the comparison results of the associated data segment should be ignored or not. *See* Specification, page 18, lines 3-9. The extra bit, *i.e.*, the mask bit, is used by the mask circuitry 270 to facilitate selectivity of clocking-in of the data comparison results into registers 285. *See* Specification, page 18, lines 6-9. Therefore, the size of the data that is transmitted may be used to perform the decoding called for by claims of the present invention. Therefore, this is yet another example of the support for the using the size as a factor for decoding the data. The embodiments described above are merely examples of subject matter that support the claims, and as such, they do not limit the scope of the claims.

Therefore, various disclosures adequately support the various elements of the claims, including detecting the size of the data to use as a factor for decoding the data, and decoding the received set of data. Therefore, claims 1, 10, 23, 32, and 34 are, indeed, supported by the Specification and are novel in light of the arguments provided in the Appeal Brief and this Response.

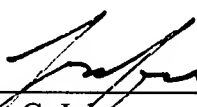
Applicant respectfully asserts that in light of the amendments and arguments provided by Applicant throughout the prosecution of the present application, all claims of the present application are now allowable and, therefore, request that a Notice of Allowance be issued. In light of the above arguments, reconsideration of the present application is respectfully requested.

If for any reason that this application is deemed to be other than in condition for allowance, **it is respectfully requested that the undersigned attorney be contacted** at the

Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,  
WILLIAMS, MORGAN & AMERSON, P.C.

Date: August 17, 2007



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